ROBUST GaAs MMIC AMPLIFIERS USING PLANAR ION-IMPLANTED POWER MESFETS WITH IMPROVED OPEN-CHANNEL BURNOUT

D.C Miller, R. A. Sadler, and A. H. Peake

ITT GaAs Technology Center
Roanoke, VA 24019

ABSTRACT

Planar ion-implanted GaAs MESFETs with modified drain n^+ regions show increased open-channel burnout voltage, making them robust against transient overvoltages. This increases circuit yields through pulsed on-wafer testing from < 50% to ~ 90%. Higher drain biases can also be used, allowing 9 W of output power to be produced with V_{DS}=13V by an X-band MMIC amplifier designed to produce 4 W with V_{DS}=7V.

INTRODUCTION

When testing FET power amplifiers, transients in the output of the RF signal source can cause inductive ringing which adds to the applied dc gate and drain biases. Momentary transient voltages may exceed the device's burnout voltage, leading to device failure. By modifying the drain n^+ implant structure of our planar ion-implanted GaAs MESFETs, we have increased their open-channel burnout voltage significantly, making them much more robust against such transient overvoltages. We have also found that the modified FETs can be operated with higher drain bias, which greatly increases their output power.

DEVICE MODIFICATION

Fig. 1(a) shows a cross-section of a conventional planar power MESFET. The channel has a buried-*p* layer below the n-type implant to give a sharper pinch-off characteristic. Ion-implanted source and drain regions are used, with the drain region spaced further from the gate to increase the gate-drain breakdown voltage. Fig. 1(b) shows the burnout characteristics of this device obtained by burning out identical devices with different gate-source biases applied. The open-channel burnout voltage (V_{DS}) is ~ 13 V. Fig. 2(a) shows a cross-section of a modified device which includes a lightly-doped guard region between the drain n+ region and the rest of the device. Fig. 2(b) shows the burnout characteristics of this device. The open-channel burnout voltage is ~ 20 V for the modified device.

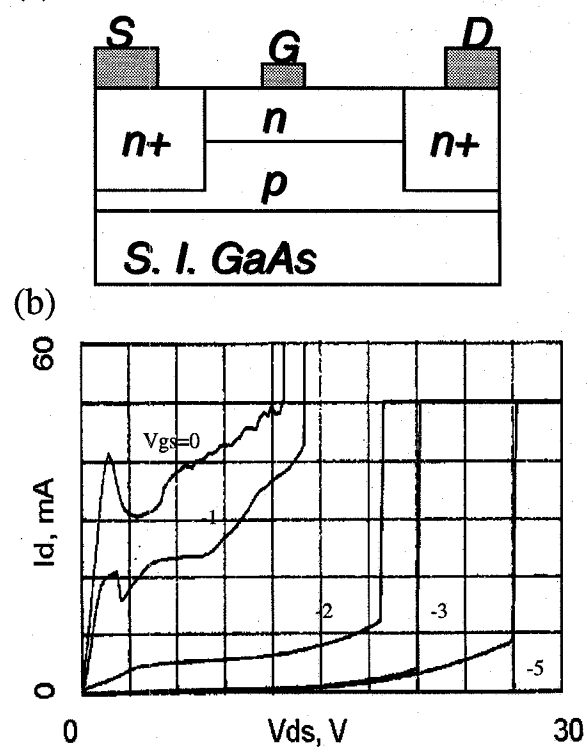

Fig. 1. *Cross-section (a) and burnout characteristics (b) of standard ion-implanted planar power MESFET device.*

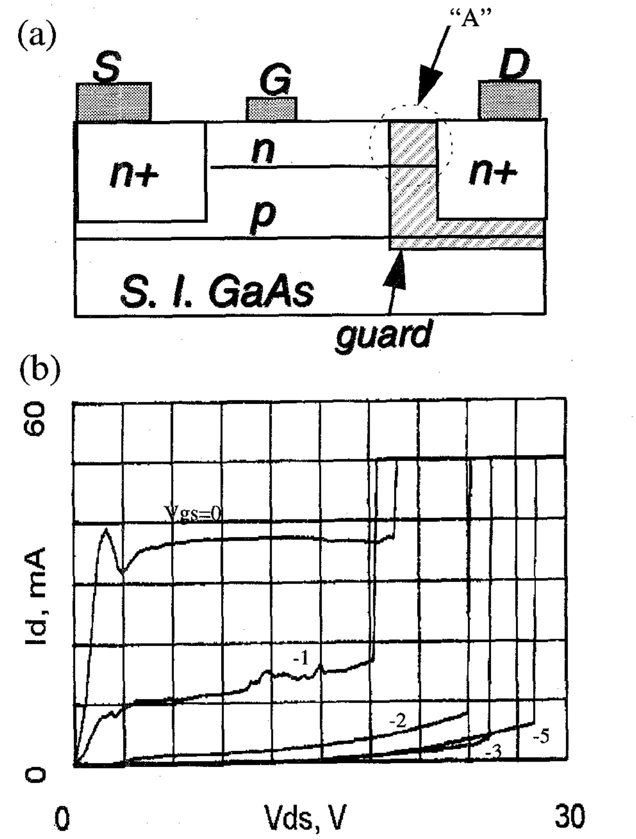

Fig. 2. *Cross-section (a) and burnout characteristics (b) of modified planar ion-implanted GaAs power MESFET device.*

Modeling of the dopant profiles for the channel, n^+, and buried-p implants (same in both devices) and the guard implant (present only in the modified device) suggests that the guard implant does not alter the doping in the region marked "A" in Fig. 2(a) significantly. However, it does have a large effect on the n^+/p junction which occurs below region "A" at the edge of the drain n^+ region. The observed improvement in burnout implies that the site at which avalanche breakdown occurs under open-channel conditions in the standard device is not the corner of the gate closest to the drain or in the channel itself (since these regions are the same in both devices), but below the channel at the n^+/p junction.

DC AND SMALL SIGNAL RESULTS

Because the site of open-channel avalanche breakdown was not in the active channel, we have been able to increase the open-channel burnout voltage without having much effect on other device characteristics. As shown in Tables 1 and 2, both dc parameters and small-signal equivalent circuit parameters are very similar for devices with and without the modification.

Table 1. *DC parameters (wafer means) from devices without and with the additional guard region.*

Parameter	w/o guard	w/guard
Ipeak, mA/mm	394.9	412.4
Idss, mA/mm	323.8	323.7
Vt, V	-2.5	-2.1
Gm @ 50% I_{DSS}, mS	187.7	183.1

Table 2. *AC small-signal equivalent circuit parameters fit to S-parameters measured from 0.5 - 18 GHz on 300 μm wide devices biased at* $V_{DS} = 3$ *V,* $I_D = 50\% I_{DSS}$.

Parameter	w/o guard	w/guard
gm, mS	51.2	52.6
Cgs, fF	454.8	496.1
Cgd, fF	24.3	29.6
Cds, fF	72.7	71.6
Rds, ohms	362.2	364.6

RESISTANCE TO TRANSIENT BURNOUT

Evidence for increased robustness against transient overvoltage conditions is shown in Table 3. Circuit yield through a particular on-wafer pulsed RF test was found to be < 50% on C-band 4 W amplifier MMICs made with standard devices. Although the applied dc voltages and expected RF excursions were well within the limits indicated in Fig. 1(b), transients measured during turn-on or turn-off showed the actual drain voltage peak to be as high as 20 V, enough to cause device failure in the open-channel condition. As shown in the table, circuits made with improved devices showed more than twice the yield through the same test.

Table 3. *Circuit yield (survival) through on-wafer pulsed power test (C-Band 4 W amplifier MMIC).*

Wafer	Process	% surviving
1	w/o guard	56
2	w/o guard	48
3	w/o guard	27
4	w/o guard	34
average	w/o guard	42
5	w/ guard	89
6	w/guard	89
7	w/ guard	88
8	w/ guard	94
9	w/guard	89
average	w/guard	90

OPERATION AT HIGHER DRAIN BIAS

The observed increase in open-channel burnout also allows the modified devices to be operated with a larger drain bias to get more power. Fig. 2 shows output power obtained from an X-band 4 W amplifier as a function of drain bias. At $V_{DS} = 7$ V, (the design value), the output power is 35.3 dBm (3.4 W). When the drain bias is increased to 13 V, the output power increases to 39.5 dBm (9 W). Devices without the improvement typically burn out when V_{DS} is increased above 9 V. With the burnout improvement, devices have been operated with $V_{DS} >$ 20 V before burning out.

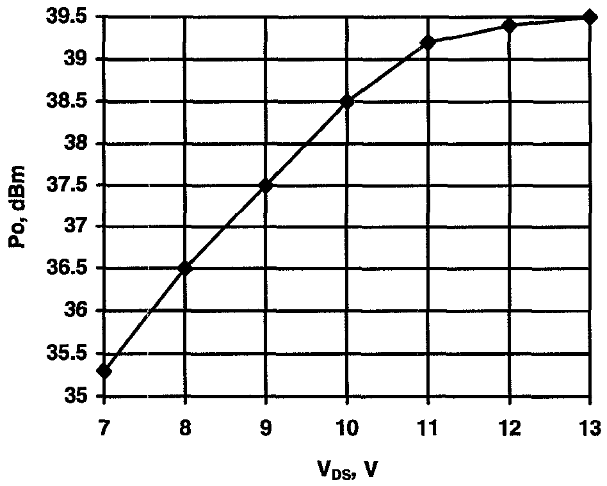

Fig. 2. *Output power at 1 dB compression point at 9 GHz for a (nominal) 4 W X-band amplifier as a function of* V_{DS}. *Operation above* $V_{DS} = 9$ *V is not possible without the guard region.*

REFERENCES

1. A. E. Geissberger, I. J. Bahl, E. L. Griffin, and R. A. Sadler, "A New Refractory Self-Aligned Gate Technology for GaAs Microwave Power FET's and MMIC's," *IEEE Trans. on Electron Devices,* vol. 35, pp. 615-622, May 1988